In The Claims

Applicants submit below a complete listing of the current claims, with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing.

Listing of the Claims

1. (Currently Amended) An integrated circuit including a vertical power component having a terminal formed by a chip substrate of a first conductivity type, a control circuit thereof, the control circuit isolated from the substrate by means of an isolation region of a second conductivity type, and a protection structure against polarity inversion of a substrate potential comprising a first bipolar transistor with an emitter connected to said isolation region and a collector connected to a reference potential input of the integrated circuit, the reference potential input providing a reference potential, a bias circuit for biasing the first bipolar transistor in a reverse saturated mode when the substrate potential is higher than the reference potential, and a second bipolar transistor with an emitter connected to the substrate and a base coupled to the isolation region for coupling the isolation region to the substrate through a high-impedance when the substrate potential is lower than the reference potential and the first bipolar transistor is off.

2. (Original) An integrated circuit according to claim 1, wherein said bias circuit comprises a third bipolar transistor with an emitter coupled to control terminal of the integrated circuit and a collector coupled to a base of the first bipolar transistor, said control terminal receiving an external control signal which is used by the control circuit to cause switching of the power component, said control signal being used to provide a voltage supply to the control circuit and to the bias circuit.

3. (Previously Presented) An integrated circuit according to claim 2, wherein said first bipolar transistor is a vertical transistor having an emitter formed by said substrate, a collector formed by a second doped region of the first conductivity type, and a base formed by a first doped region of the second conductivity type formed in the substrate and within the first doped region.

4. (Previously Presented) An integrated circuit according to claim 3, wherein said first and third bipolar transistors are isolated from the substrate by said isolation region.

5. (Original) An integrated circuit according to claim 4, wherein said first conductivity type is the N type, said second conductivity type is the P type, said first and second bipolar transistors are NPN transistors, and said third bipolar transistor is a PNP transistor.

6. (Original) An integrated circuit according to claim 1, wherein said vertical power component is a vertical power bipolar transistor.

7. (Currently Amended) A semiconductor device, comprising:

(A) a vertical power component having a terminal formed by a substrate of a first conductivity type;

(B) a control circuit, isolated from the substrate by an isolation region of a second conductivity type; and

(C) a protection structure against polarity inversion of a substrate potential, comprising:

(i) a first bipolar transistor having an emitter connected to said isolation region and a collector connected to a reference potential input of the integrated circuit, the reference potential input providing a reference potential;

(ii) a bias circuit that biases the first bipolar transistor in a reverse saturation mode when the substrate is at a potential higher than ~~a~~ the reference potential; and

(iii) means for coupling the isolation region to the substrate through a high impedance when the substrate potential is lower than the reference potential and the first bipolar transistor is off.

8. (Previously Presented) The device of claim 7, wherein the second bipolar transistor forms a regulation loop that reduces parasitic transistor action from affecting the first bipolar transistor and the bias circuit.

9. (Previously Presented) The device of claim 7, wherein the vertical power component comprises a vertical power bipolar transistor.

10. (Previously Presented) The integrated circuit of claim 1, wherein the first bipolar transistor couples the isolation region to the reference potential input when the substrate potential is higher than the reference potential.

11. (Previously Presented) The integrated circuit of claim 1, wherein the first bipolar transistor is off when the substrate potential is less than the reference potential.

12. (Previously Presented) The integrated circuit of claim 1, wherein the emitter of the first bipolar transistor is directly connected to the isolation region.

13. (Previously Presented) The integrated circuit of claim 1, wherein the collector of the first bipolar transistor is directly connected to the reference potential input.

14. (Previously Presented) The integrated circuit of claim 1, wherein the emitter of the second bipolar transistor is directly connected to the substrate.

15. (Previously Presented) The semiconductor device of claim 7, wherein the first bipolar transistor couples the isolation region to the reference potential input when the substrate potential is higher than the reference potential.

16. (Previously Presented) The semiconductor device of claim 7, wherein the first bipolar transistor is off when the substrate potential is less than the reference potential.

17. (Previously Presented) The semiconductor device of claim 7, wherein the emitter of the first bipolar transistor is directly connected to the isolation region.

18. (Previously Presented) The semiconductor device of claim 7, wherein the collector of the first bipolar transistor is directly connected to the reference potential input.

19. (Previously Presented) An integrated circuit including a vertical power component having a terminal formed by a chip substrate of a first conductivity type, a control circuit thereof, the control circuit isolated from the substrate by means of an isolation region of a second conductivity type, and a protection structure against polarity inversion of a substrate potential comprising a first bipolar transistor with an emitter connected to said isolation region and a collector connected to a reference potential input of the integrated circuit, a bias circuit for biasing the first bipolar transistor in a reverse saturated mode when the substrate potential is higher than the reference potential, and a second bipolar transistor with an emitter connected to the substrate and a base coupled to the isolation region for coupling the isolation region to the substrate through a high-impedance when the substrate potential is lower than the reference potential, and

wherein the emitter of the first bipolar transistor is directly connected to the isolation region.

20. (Previously Presented) A semiconductor device, comprising:

(A) a vertical power component having a terminal formed by a substrate of a first conductivity type;

(B) a control circuit, isolated from the substrate by an isolation region of a second conductivity type; and

(C) a protection structure against polarity inversion of a substrate potential, comprising:

(i) a first bipolar transistor having an emitter connected to said isolation region and a collector connected to a reference potential input of the integrated circuit;

(ii) a bias circuit that biases the first bipolar transistor in a reverse saturation mode when the substrate is at a potential higher than a reference potential; and

(iii) means for coupling the isolation region to the substrate through a high impedance when the substrate potential is lower than the reference potential,

wherein the emitter of the first bipolar transistor is directly connected to the isolation region.